



Revolutionary Web Based NPD Management System

IC design best practices, work flow,
checklists, status, templates and
repository all in one simple web based
environment.

Execution Challenges

- **Overall Projects across multiple industries:**
 - Organizations spent \$346 Billion on projects in 2006. Only 35% were successful, whereas, 46% were challenged and 19% failed. For very large projects, 39% failed.
 - The Standish Group
- **IC Design:**
 - **Business Perspective: Cycle time --> Time to Revenue**
 - Faster, cheaper and predictable (on schedule)
 - **Design Perspective: Inadequate Tools**
 - Complex interdependencies of tools, they don't all work well together
 - **Jorvig's Perspective: Non-optimal team member knowledge of detailed expectations**
 - Best Practices, design process, unknowns and deliverables.
 - Process will bring significant benefit to execution excellence.

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Ideal Success Goal for a NPD Effort

Who and
when
typically
done well

What, where
and **how** is
the
challenge
area

Everyone on the product development team will know **what** they are delivering, **when** it's expected to be delivered, **how** it's being delivered, **who** they are delivering it to and **where** it's being delivered for every item they are responsible for. Conversely, every member of the team will know **what** they are receiving, **when** they expect to receive it, **how** it will be delivered to them, **who** is delivering it and **where** it will be delivered to them for every item they will be receiving.

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Process Solution Requirements

- **Enable simple knowledge transfer of deliverable expectations.**
- **Consistent approach and deliverables shared by everyone.**
 - Improve the clarity of the deliverable what, how and where.
- **Work flow expectations highly accessible and updatable by entire team.**
- **Design knows what PE, TE, PM & Marketing needs from them. *Always!***
- **PE, TE, PM & Marketing knows what design needs from them. *Always!***
- **Solid understanding by everyone of what's done, what needs to be done and where the problems are.**

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The Solution Platform



Process Management & Governance Company

***Online framework for
creating, implementing, and
reusing best practices***

Version 11/28/07-1

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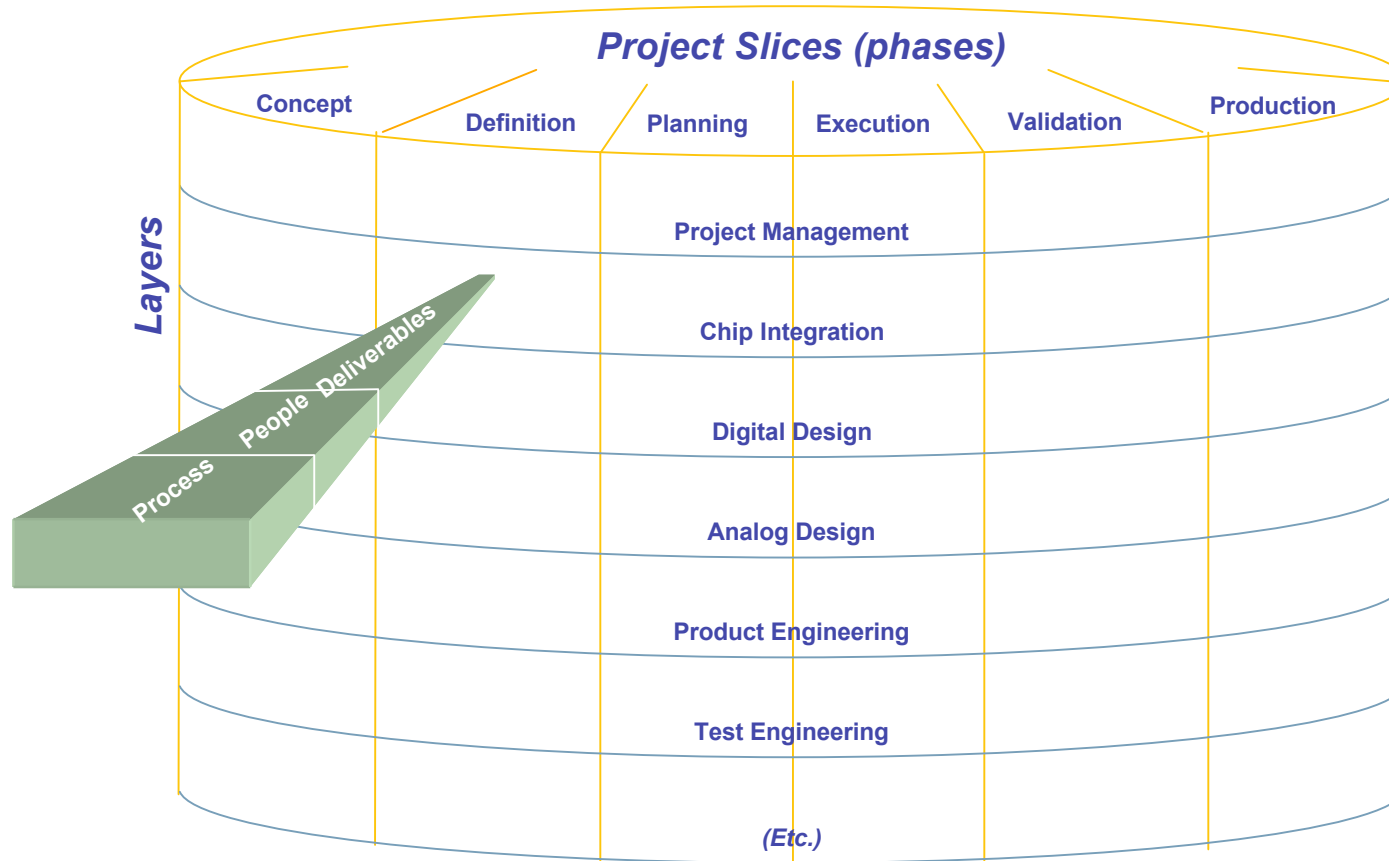


The PIEmatrix Advantage

- **Everyone on the same page, doing the same things the same way.**
- **Everyone knows what to do, what is to be delivered and where to find it... on their own.**
- **Automation of the entire NPD process and the required paper trail.**
- **Tracking the progress in real-time and ensuring compliance to previously developed and approved practices.**
- **It's a checklist, tracking, repository, best practices and flow management tool all in a unique user web based interface to simplify the whole process.**

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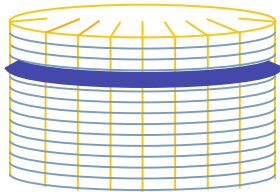
PIE Slices & Layers for a Project



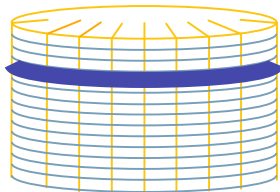
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All Like Type Designs Follow Same Process

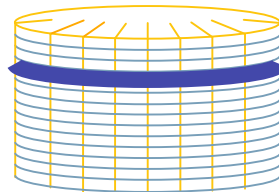
Chip A



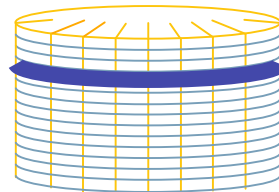
Chip B



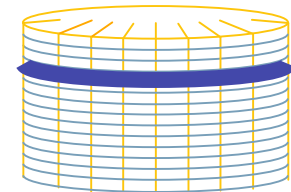
Chip C



Chip D



Chip E

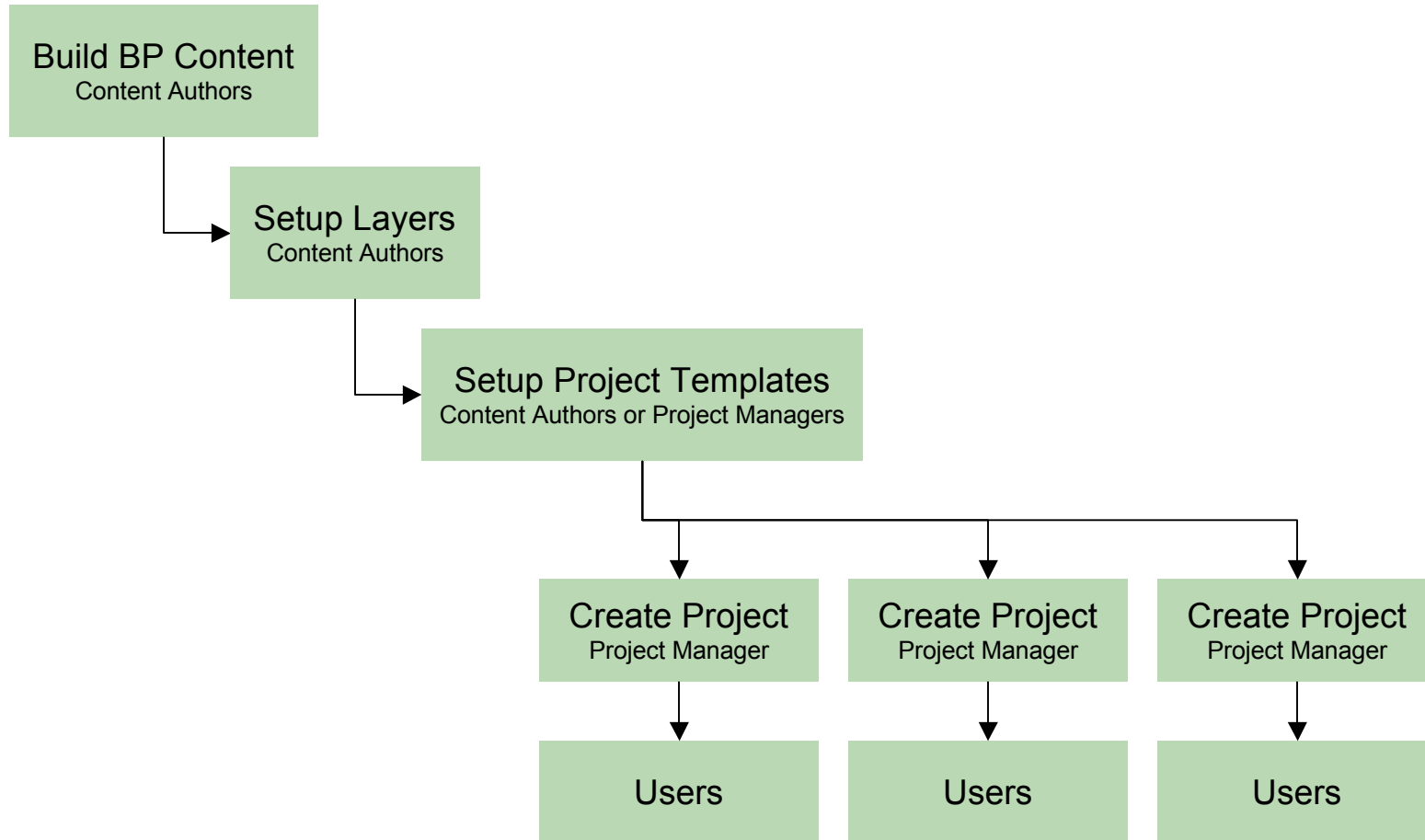


**Different processes, practices and layers are established
for each type of chip via a specific pre-configured
template set.**

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Authoring & Setup in PLEmatrix



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Chip Project Update View

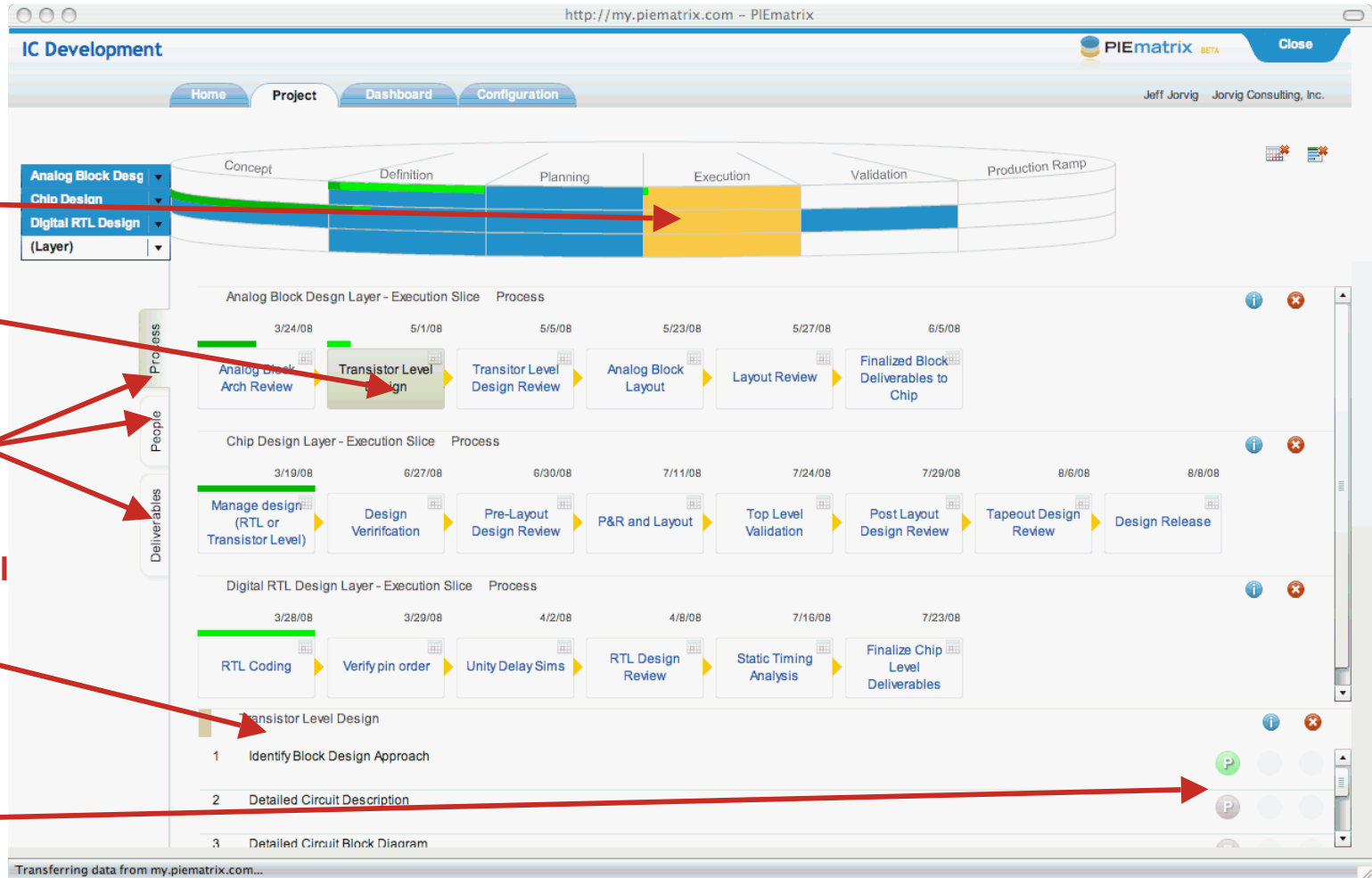
Selected Phase & layer View

Process group within layer

Process group view tabs

Task/people/deliverables details within process group

Individual task updates



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IC Development

PIEmatrix BETA

Home Project Dashboard Configuration

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Concept Definition Planning Execution Validation Production Ramp

Analog Block Design Layer - Execution Slice Process

3/24/08 5/1/08 5/5/08 5/23/08 5/27/08 6/5/08

Analog Block Arch Review Transistor Level Design Transistor Level Design Review Analog Block Layout Layout Review Finalized Block Deliverables to Chip

Chip Design Layer - Execution Slice Process

3/19/08 6/27/08 6/30/08 7/11/08 7/24/08 7/29/08 8/6/08 8/8/08

Manage design (RTL or Transistor Level) Design Verification Pre-Layout Design Review P&R and Layout Top Level Validation Post Layout Design Review Tapeout Design Review Design Release

Digital RTL Design Layer - Execution Slice Process

3/28/08 3/29/08 4/2/08 4/8/08 7/16/08 7/23/08

RTL Coding Verify pin order Unity Delay Sims RTL Design Review Static Timing Analysis Finalize Chip Level Deliverables

Transistor Level Design

- Identify Block Design Approach
- Detailed Circuit Description
- Detailed Circuit Block Diagram

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Process/Practices Setup View

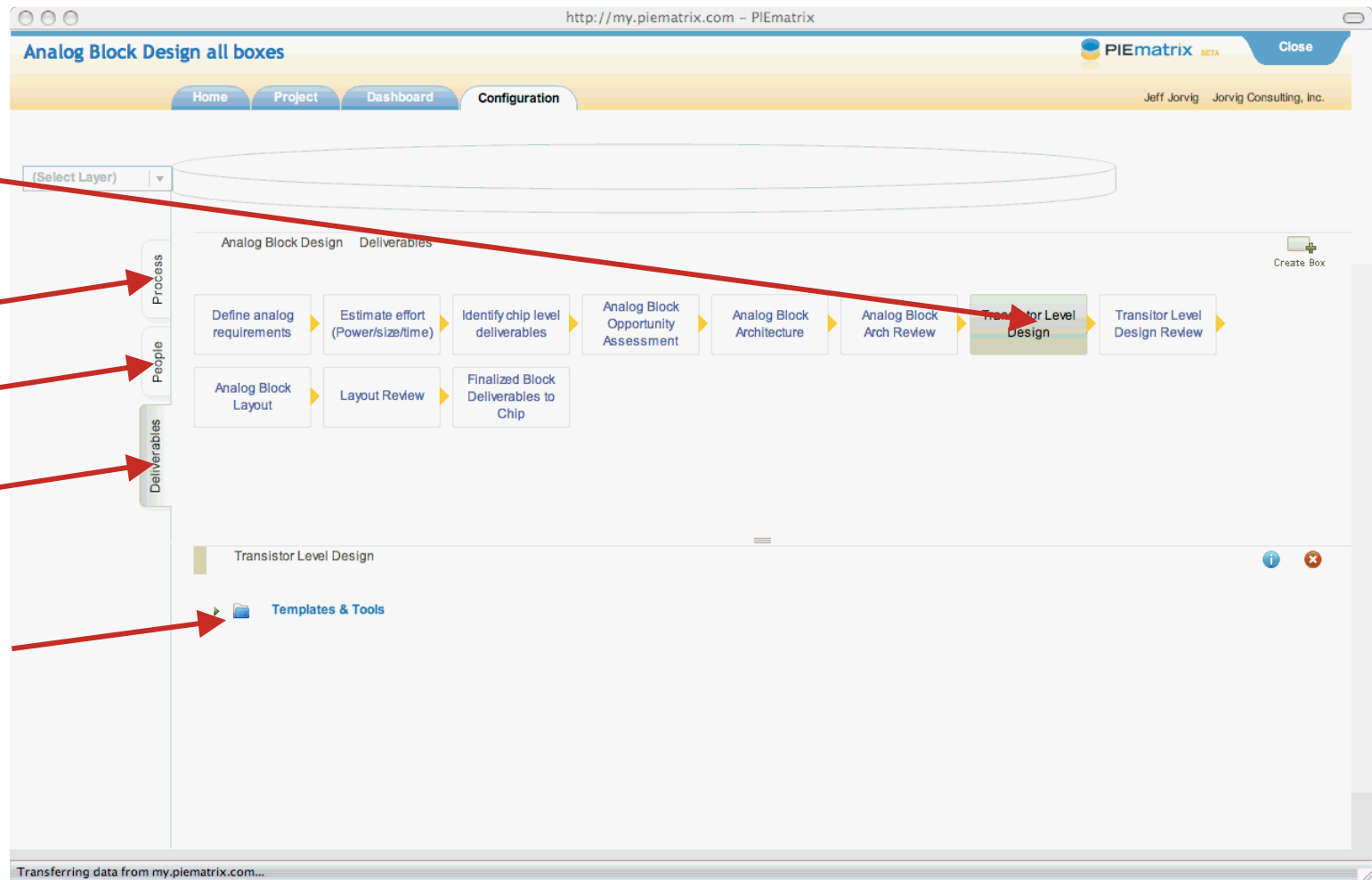
Create process group

All Tasks for group

All People for group

All deliverables for group

All doc templates for a process group here



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Analog Block Design all boxes

PIEmatrix BETA Close

Home Project Dashboard Configuration

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(Select Layer)

Analog Block Design Deliverables

Create Box

Define analog requirements Estimate effort (Power/size/time) Identify chip level deliverables Analog Block Opportunity Assessment Analog Block Architecture Analog Block Arch Review Transistor Level Design Transistor Level Design Review

Analog Block Layout Layout Review Finalized Block Deliverables to Chip

Transistor Level Design

Templates & Tools

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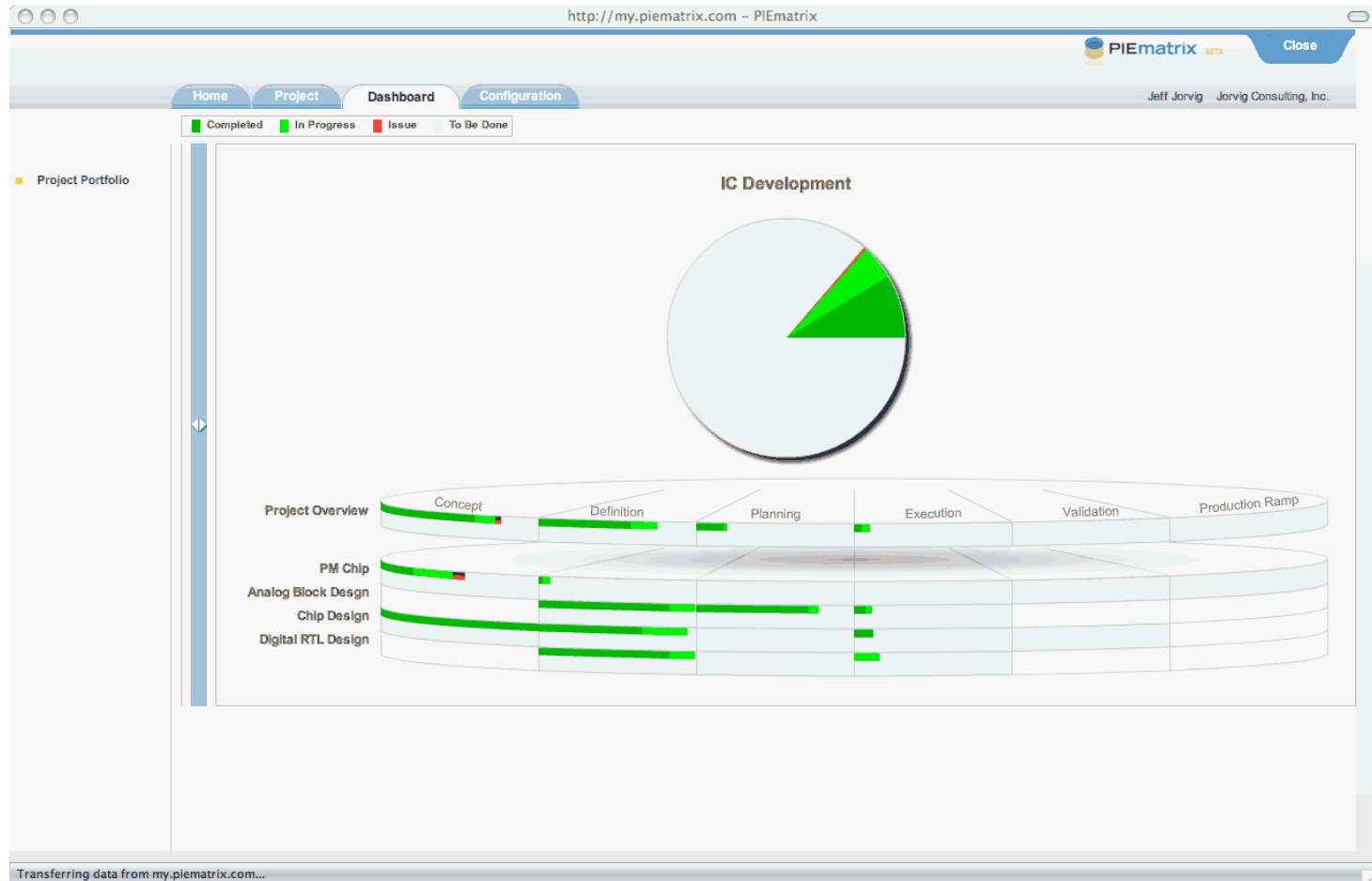


Project Status View

Dark green shows completion

Light green shows in progress

Red shows issues. Hover over for details



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Interested in Learning More?

I look forward to showing you a demo of this revolutionary system for semiconductor NPD projects.

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