

BLOCK GUIDE

ANALOG BLOCK DESIGN GUIDE TEMPLATE



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1 BACKGROUND INFORMATION

1.1 BLOCK GUIDE OVERVIEW

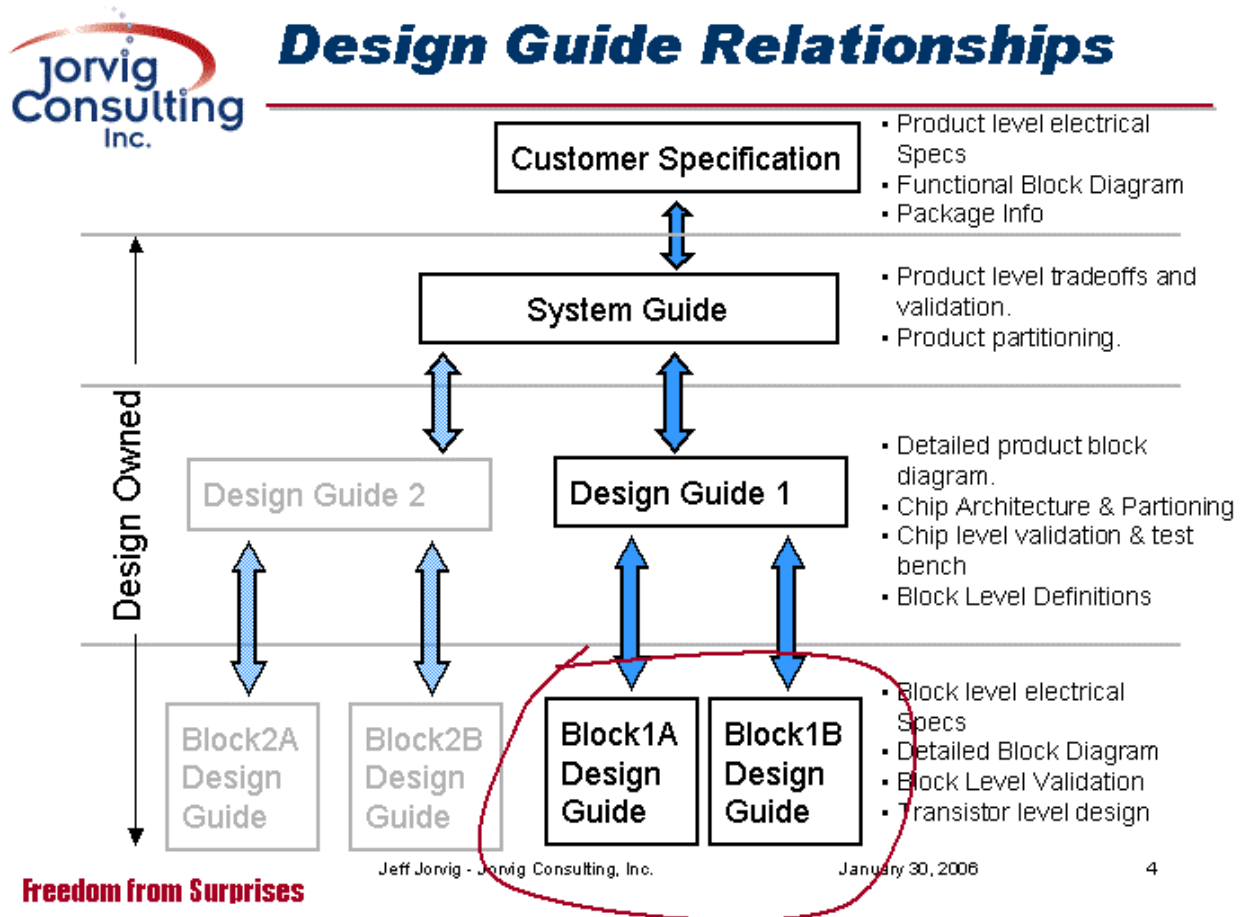


Figure 1-1: Design Guide Hierarchical Relationships

The block design guide is the lowest level in the family of hierarchical documents for managing the design process on a project. As identified in the figure above you can see the relationship of the block guide document to the higher level documents for the chip and system activities. Each level of the guide will have sections containing information to be passed down from the higher-level activities. As an example, the block level guide has an architectural section within it that is to be completed by the individual responsible for the chip architecture. View this is the requirements information being passed from the architect down to the transistor level designer. Another point of view would be that the architecture section contains “instructions” from the chip architect to the block level designer.

1.1.1 GUIDE USER INPUT AREAS

Areas within the guide that are enclosed within <> contain information that is used to describe the information requirements for a given section. This information may be removed as each section is completed.

1.2 BEST PRACTICES

<General information about the project best practices should be entered here. If there is a best practices document for the project add a link to that document in this section.>

- Project Setup Name = ????

1.3 FAB PROCESS OPTIONS

<Any unique information about the process should be covered in this section.>

- Baseline Process = ?????
- Number of poly layers = ????
- Number of metal layers = ????

1.4 DEFINITION OF TERMS

Term	Definition
Architecture	The partitioning of a system, design or block into its next lower level of functions.
ATPG	Automatic Test Program Generation
BLM	Behavioural Level Model. This is a high level model of a system, chip or a block.
Block Guide	The detailed design document for each of the blocks within a design.
Chip	A single silicon die comprised of multiple functional blocks.
DFT,DFA,DFR	Design for Test, Design for Assembly, Design for Reliability
Stimulus	The input to a simulation. This can be digital test vectors, data tables or Spice signal descriptions.
System	The top most definition of a design and is typically comprised of multiple chips.
Test Bench	The simulation environment for a system, chip or block.

Table 1-1: Definition of Terms

2 BLOCK OPPORTUNITY ASSESSMENT

This section covers the activities associated with the early assessment and feasibility activities for an IP block to be used on a project. This section is to be filled out by the individual responsible for the assessment activities that will feed into the business opportunity analysis.

2.1 BLOCK FUNCTION SCOPE

<Describe the scope of functionality for the block. Cover the operation requirements for the block in relation to meeting the chip objectives. Include any anticipated risk areas such as power, speed, noise immunity, size etc. Also define if there is a known starting point for the design i.e. reuse of another block either partially or in it's entirety.>

2.1.1 ADDITIONAL REUSE FUNCTIONALITY

<Identify any specific functionality requirements that are necessary for supporting possible future projects. These requirements are not specific to this particular project but have merit for a future program.>

2.2 KEY ASSUMPTIONS

<Identify any assumptions about the process, models, design environment, reusability, designer expertise or any anticipated risk areas here.>

2.2.1 SIZE ESTIMATE

<Identify how you arrived at the block size estimate identified below.>

- Block Size Estimate = ????

2.2.2 DEVELOPMENT TIME ESTIMATE

<Identify your assumptions about design and layout time here.>

- Design time in person days = ????
- Layout time in person days = ????

2.3 OPPORTUNITIES FOR RISK MITIGATION

<Describe any opportunities that may exist to reduce risk to quality, schedule etc. List the opportunities in the table below.>

Risk Mitigation Opportunity	Impact to program

Table 2-1: Risk Mitigation Opportunities